Memory cell array

(Column number)

		0	511 512	527
Block 0	Page 0	Data area(512 Bites)	Redundancy area(16 Bites)	
	Page 1			
	Page 31	NU		
Block 1	Page 0			
	Page 1			
	Page 31			
Block X	Page 0			
	Page 1			
	Page 31			

FIG. 1 (PRIOR ART)

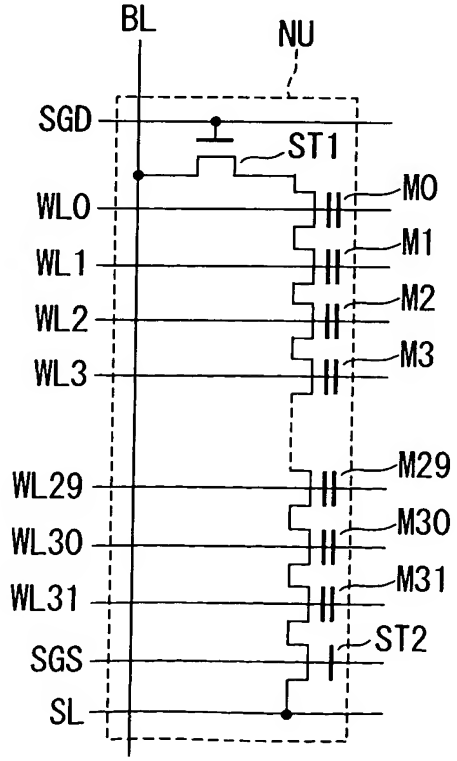

FIG. 2
(PRIOR ART)

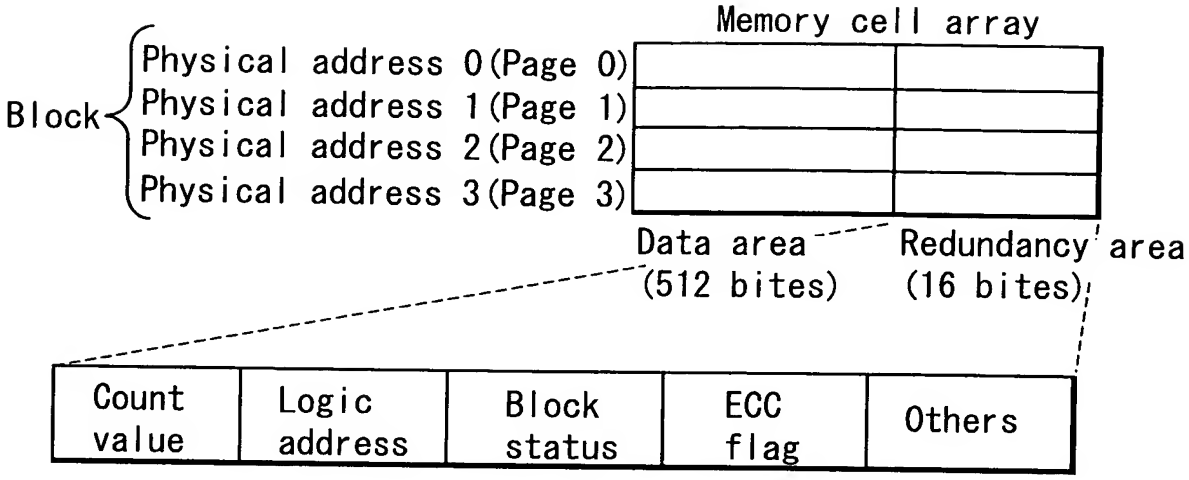
Memory cell array
Block
Physical address 0 (Page 0)
Physical address 1 (Page 1)
Physical address 2 (Page 2)
Physical address 3 (Page 3)
Data area
(512 bites)
Redundancy area
(16 bites)
Count value
Logic address
Block status
ECC flag
Others

FIG. 3

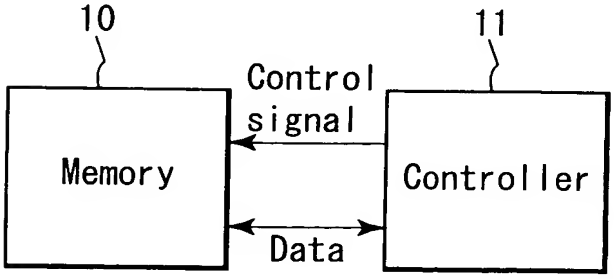
10
11
Control signal
Memory
Controller
Data

FIG. 4

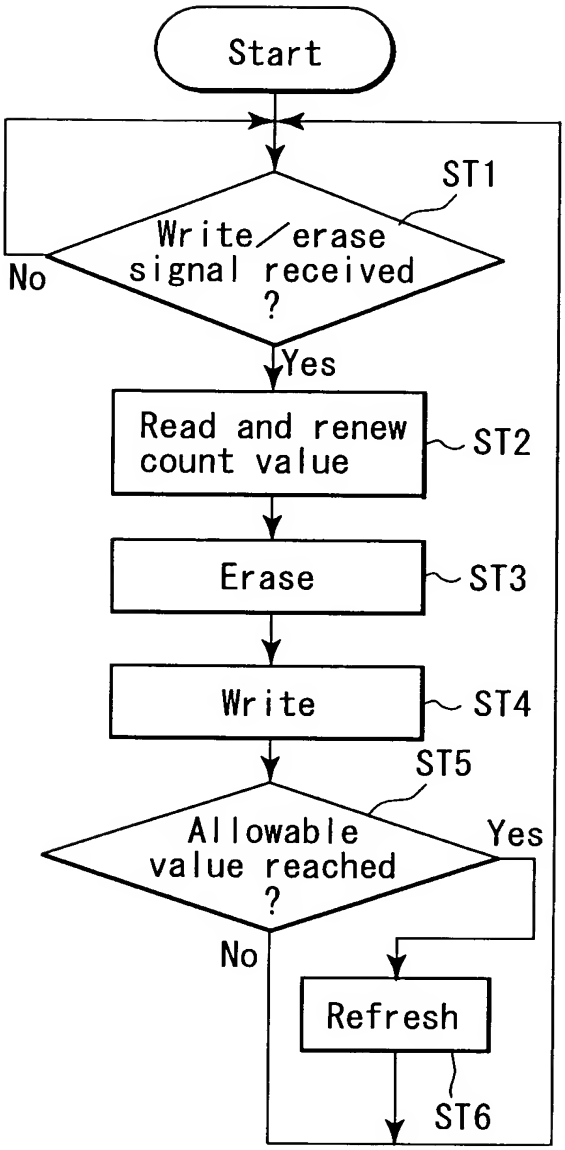
Start
ST1
Write/erase signal received ?
No
Yes
Read and renew count value
ST2
Erase
ST3
Write
ST4
ST5
Allowable value reached ?
Yes
No
Refresh
ST6

FIG. 5

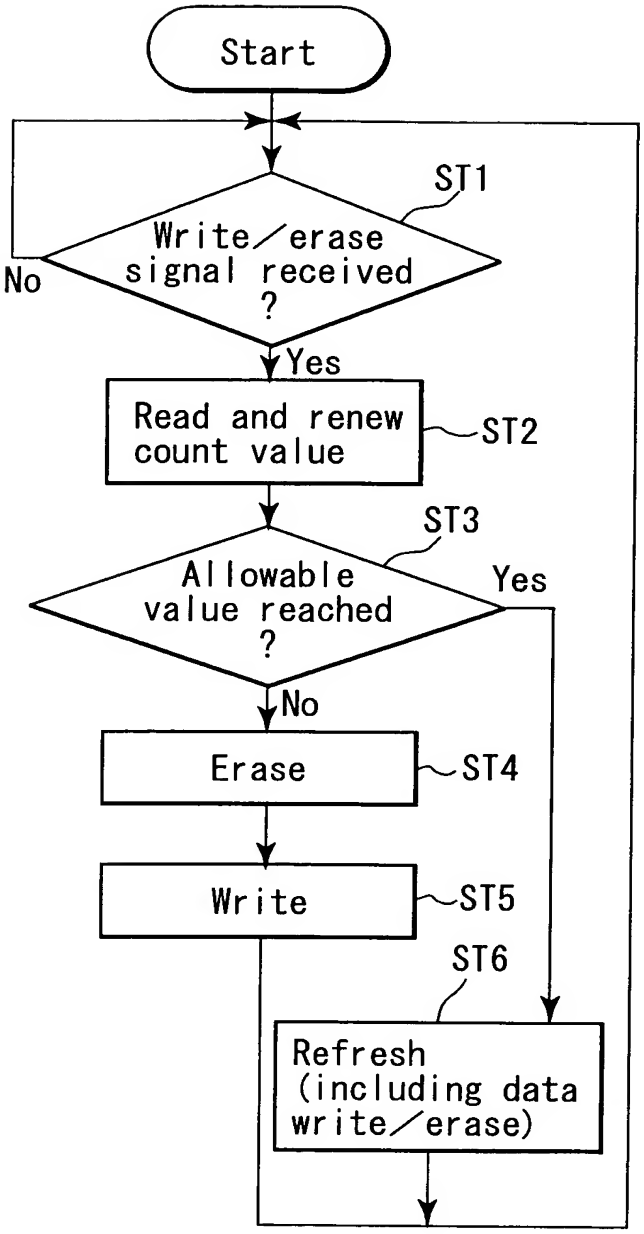
Start
ST1
Write/erase signal received ?
No
Yes
Read and renew count value
ST2
ST3
Allowable value reached ?
Yes
No
Erase
ST4
Write
ST5
ST6
Refresh (including data write/erase)

FIG. 6

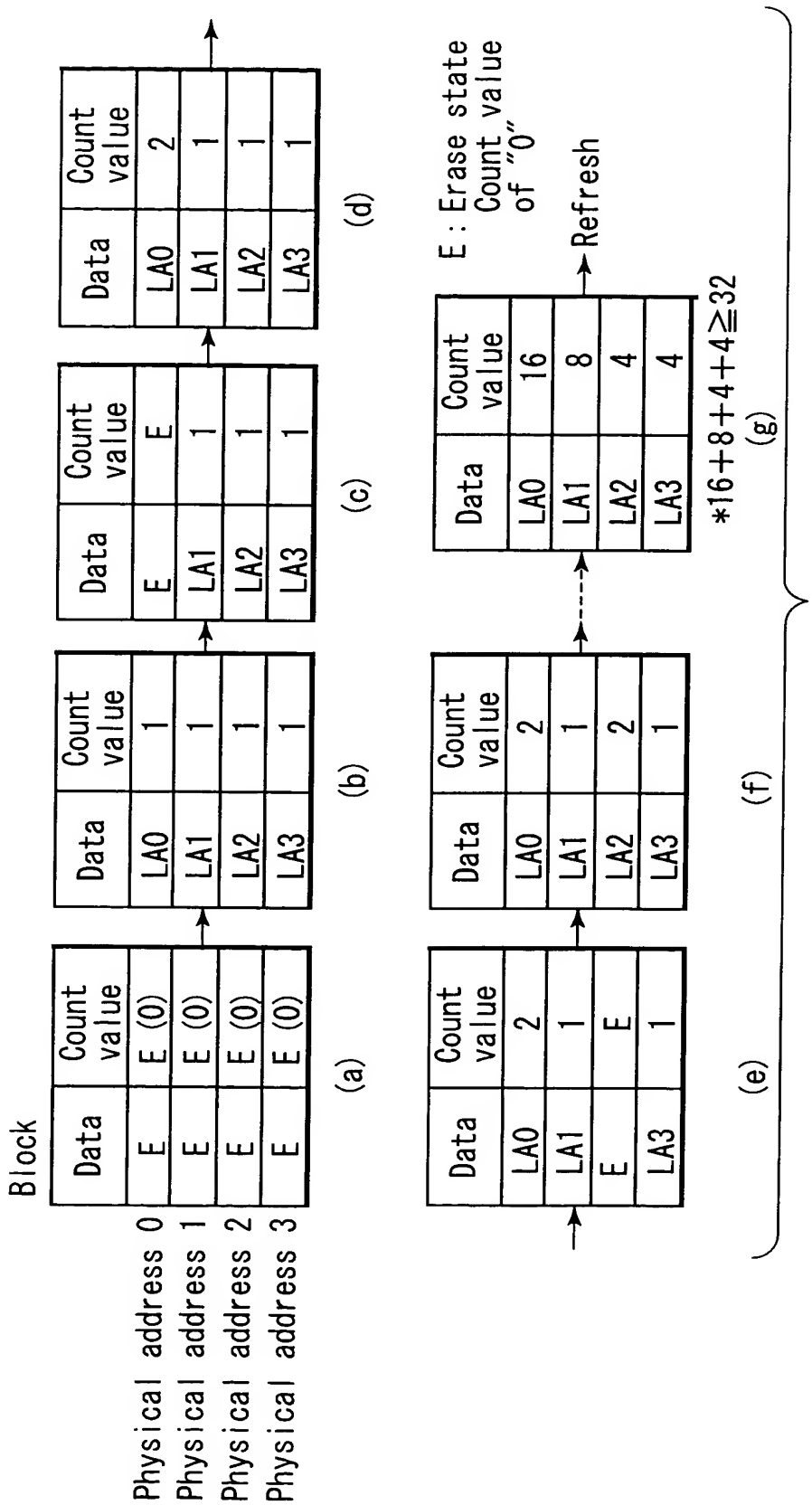
Block
Physical address 0
Physical address 1
Physical address 2
Physical address 3
Data
Count value
E
E (0)
LA0
LA1
LA2
LA3
1
2
(a)
(b)
(c)
(d)
(e)
(f)
(g)
E : Erase state
Count value
of "0"
Refresh
*16+8+4+4≧32

FIG. 7

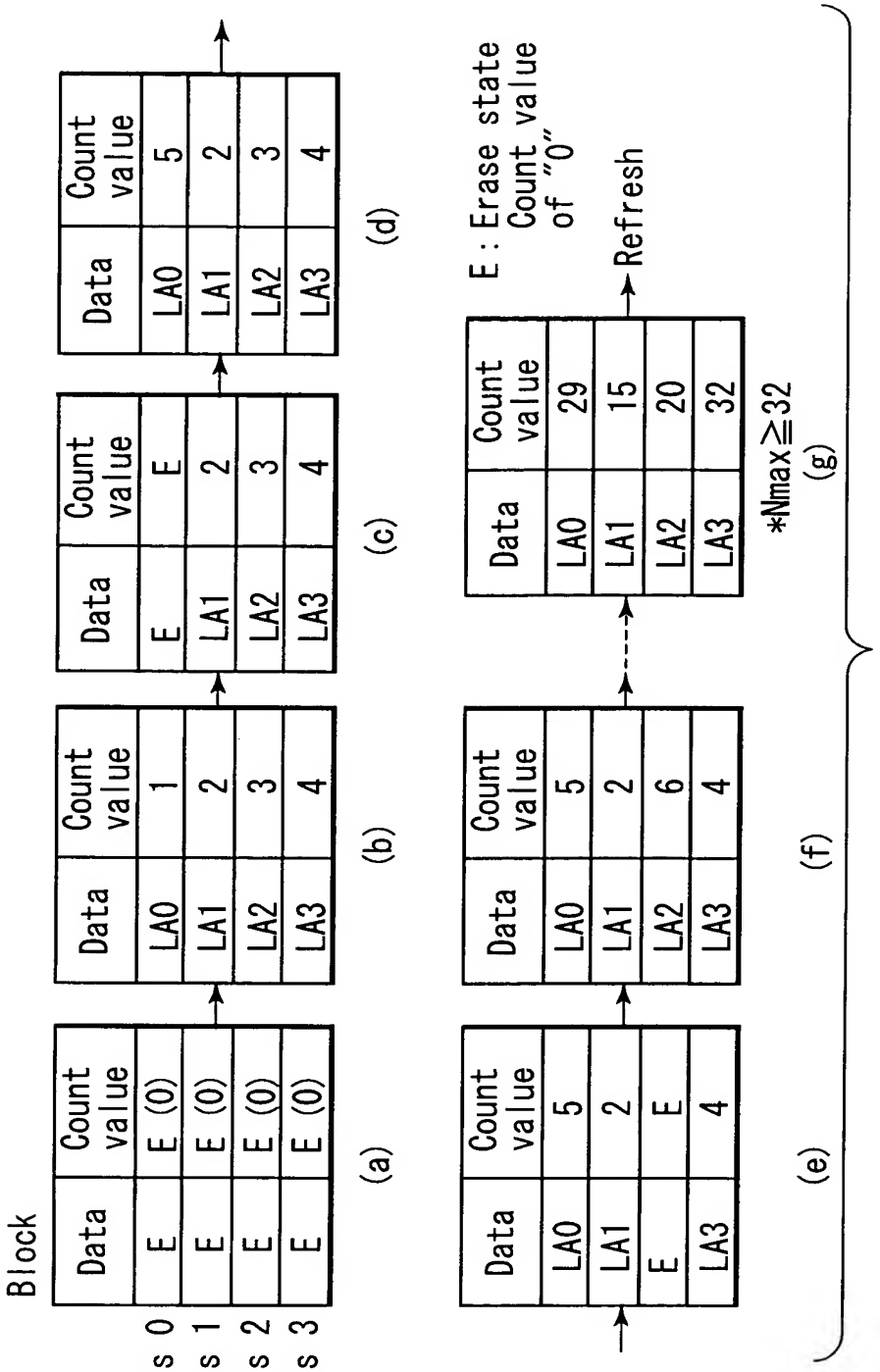
Block
Physical address 0
Physical address 1
Physical address 2
Physical address 3
Data
Count value
E
E (0)
LA0
LA1
LA2
LA3
1
2
3
4
5
6
15
20
29
32
(a)
(b)
(c)
(d)
(e)
(f)
(g)
E : Erase state
Count value of "0"
Refresh
*Nmax≧32

FIG. 8

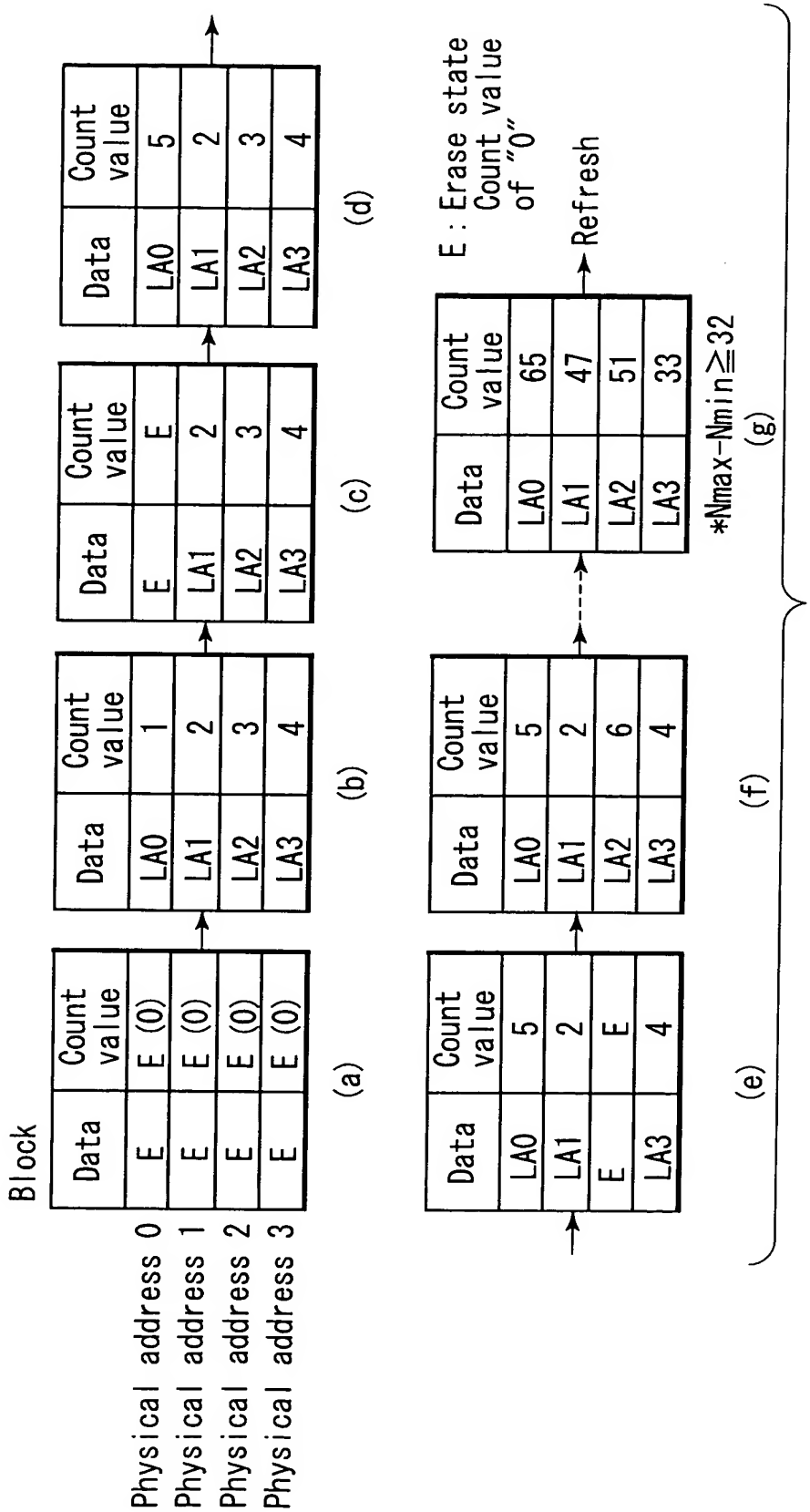
Block
Physical address 0
Physical address 1
Physical address 2
Physical address 3
Data
Count value
E
E (0)
LA0
LA1
LA2
LA3
1
2
3
4
5
6
65
47
51
33
(a)
(b)
(c)
(d)
(e)
(f)
(g)
E : Erase state
Count value
of "0"
Refresh
*Nmax-Nmin≧32

FIG. 9

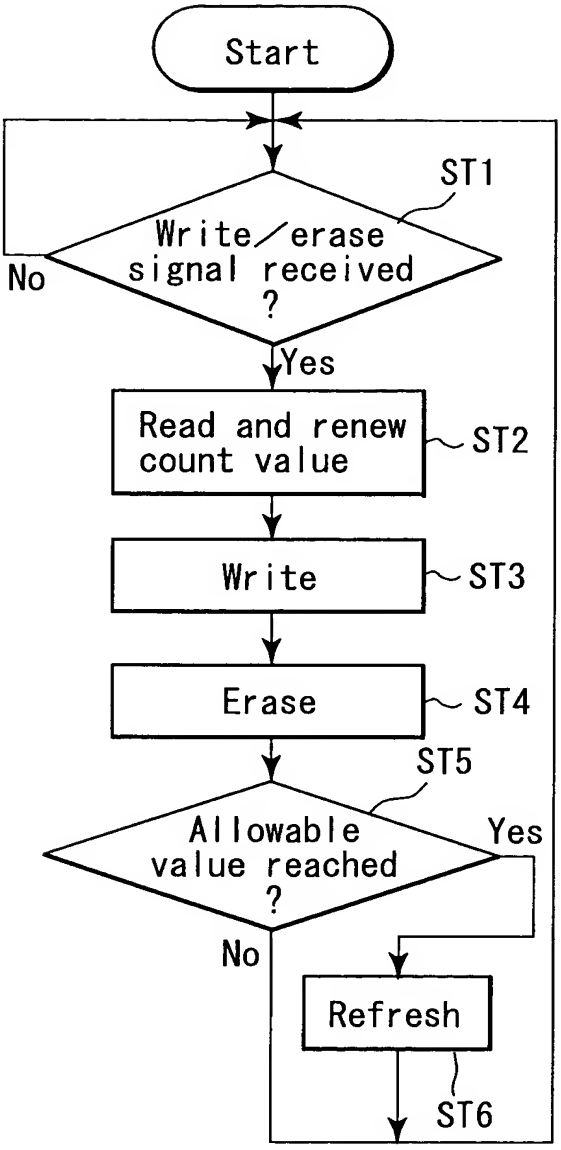
Start
ST1
Write/erase signal received ?
No
Yes
Read and renew count value
ST2
Write
ST3
Erase
ST4
ST5
Allowable value reached ?
Yes
No
Refresh
ST6

FIG. 10

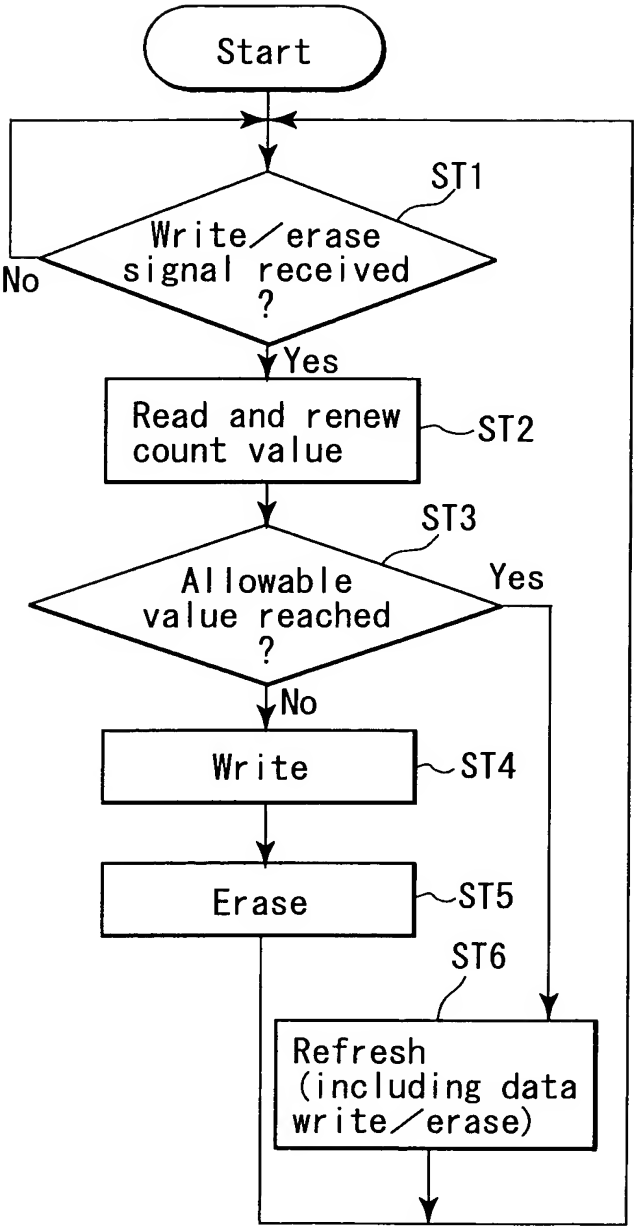
Start
ST1
Write/erase signal received ?
No
Yes
Read and renew count value
ST2
ST3
Allowable value reached ?
Yes
No
Write
ST4
Erase
ST5
ST6
Refresh (including data write/erase)

FIG. 11

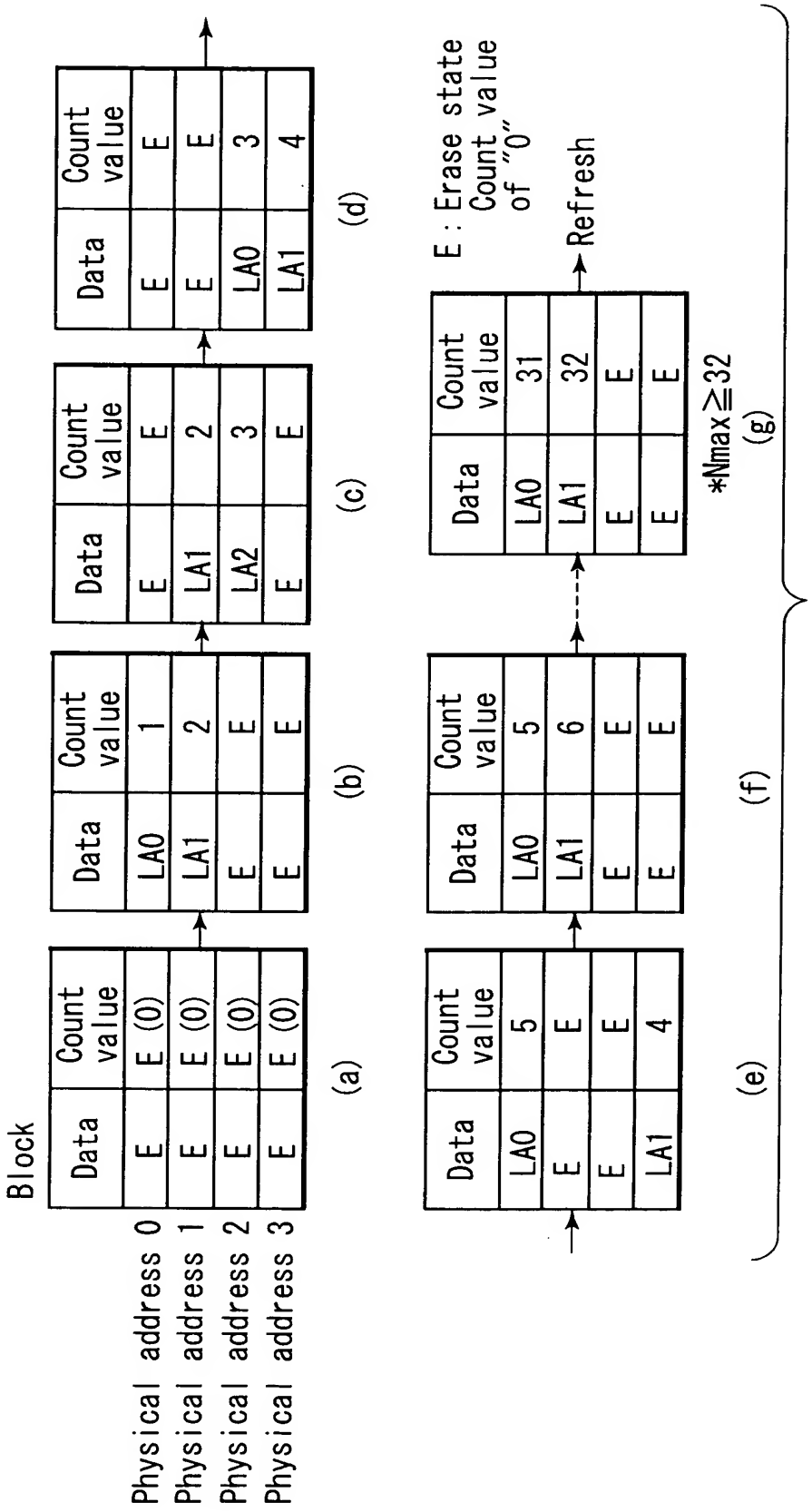
Block
Physical address 0
Physical address 1
Physical address 2
Physical address 3
Data
Count value
E
E (0)
LA0
LA1
LA2
1
2
3
4
5
6
31
32
(a)
(b)
(c)
(d)
(e)
(f)
(g)
E : Erase state
Count value
of "0"
Refresh
*Nmax≧32

FIG. 12

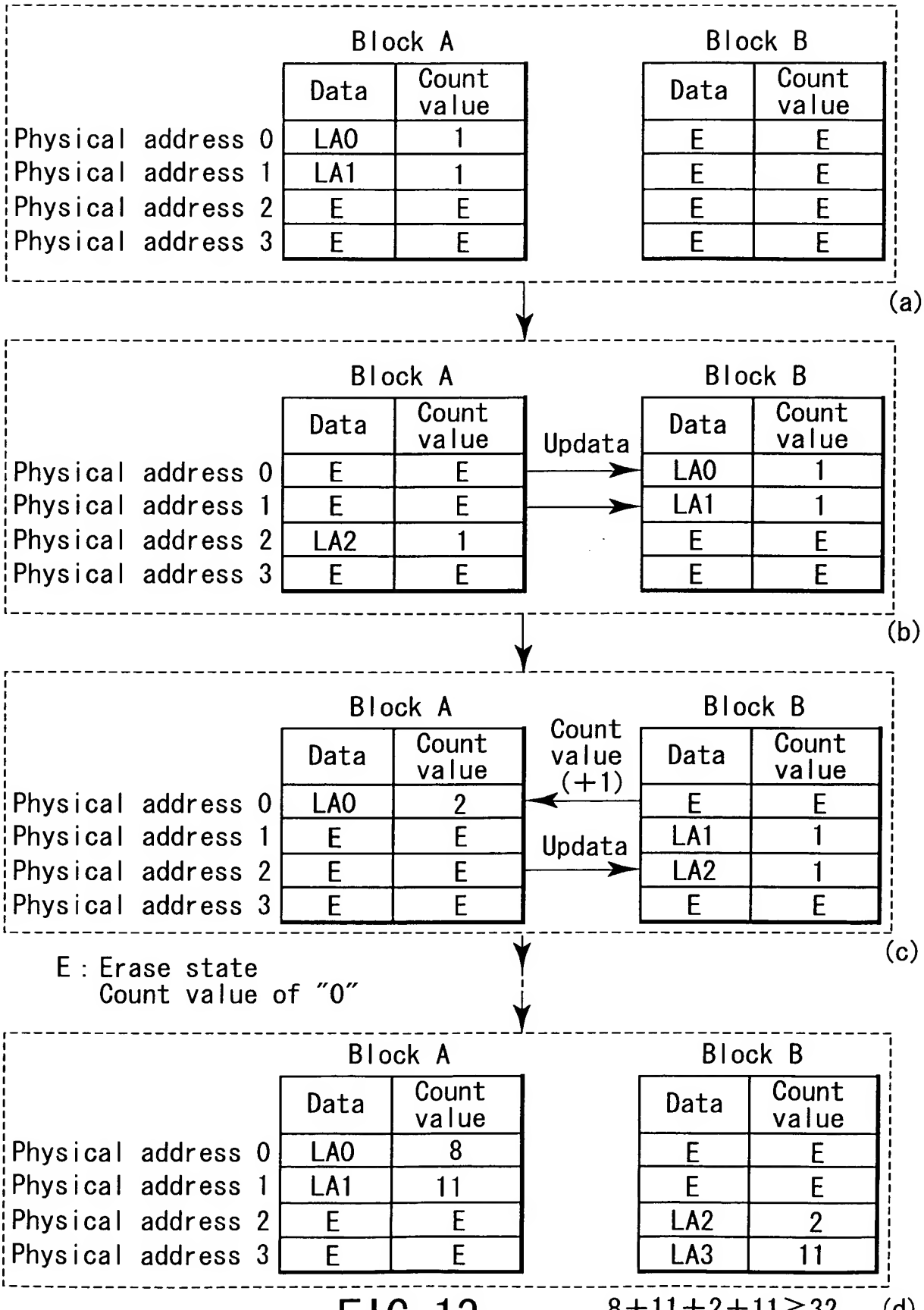
Block A
Block B
Data
Count value
Physical address 0
Physical address 1
Physical address 2
Physical address 3
LA0
LA1
LA2
E
1
2
8
11
Updata
Count value (+1)
(a)
(b)
(c)
(d)
E : Erase state
Count value of "0"
LA3
8+11+2+11≧32

FIG. 13

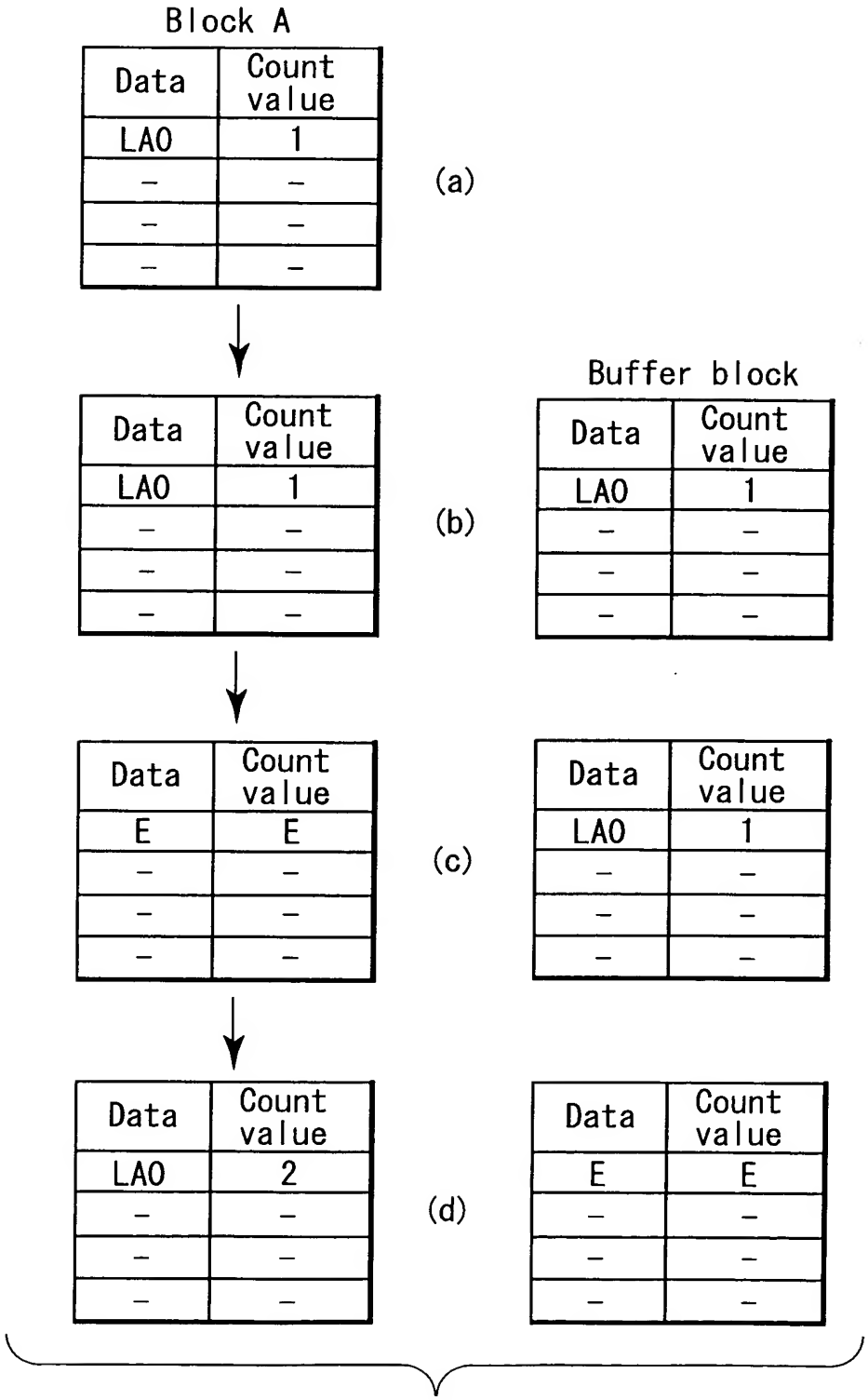

FIG. 14

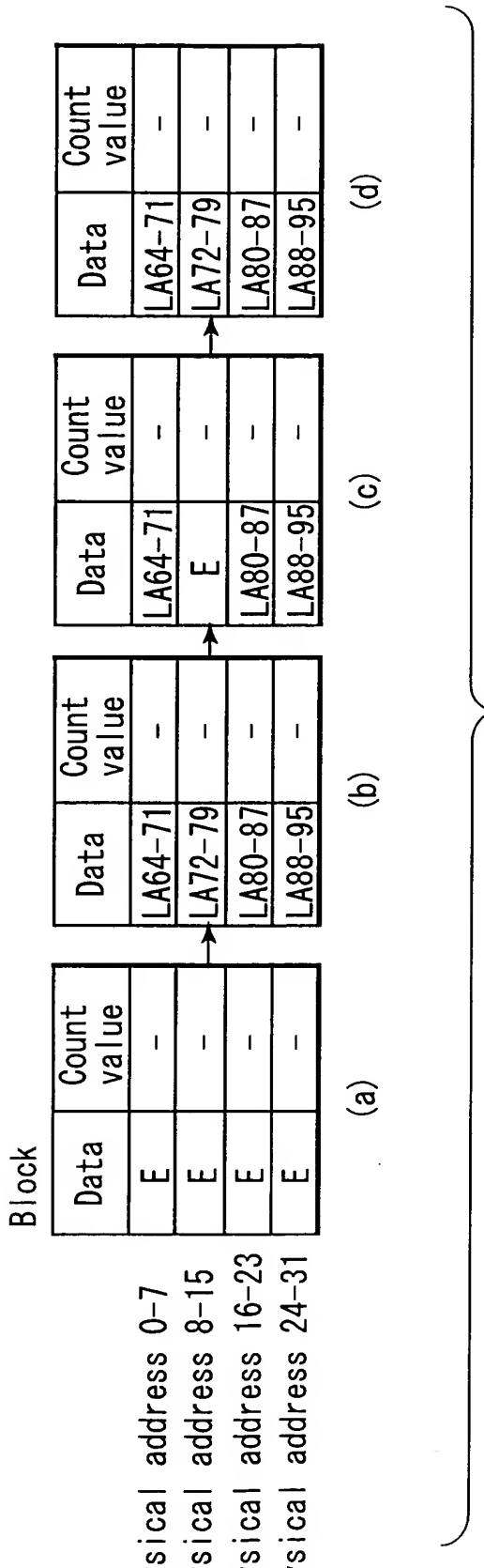
Block
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
Data
Count value
E
-
LA64-71
LA72-79
LA80-87
LA88-95
(a)
(b)
(c)
(d)

FIG. 15

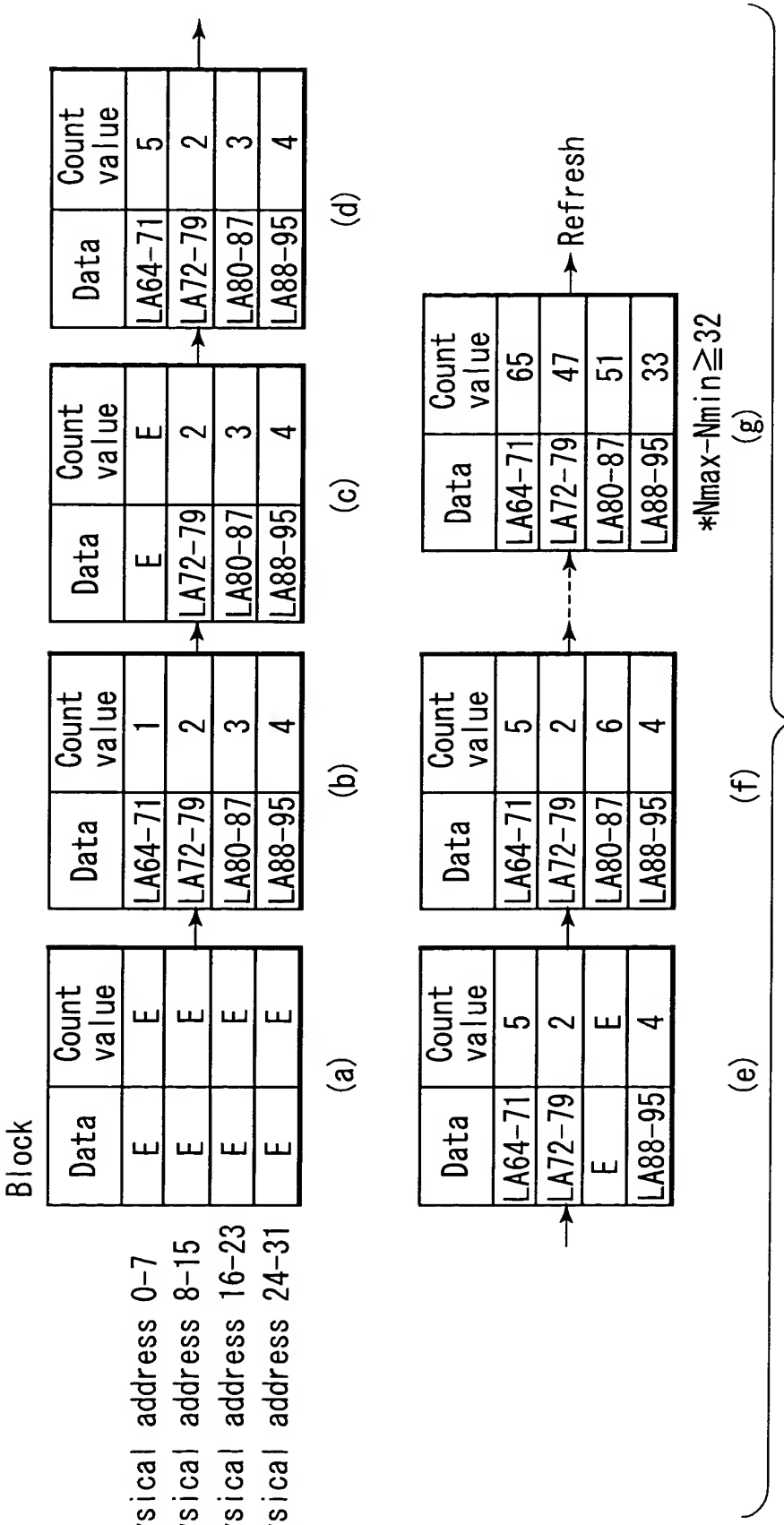
Block
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
Data
Count value
E
LA64-71
LA72-79
LA80-87
LA88-95
5
2
6
4
1
3
65
47
51
33
(a)
(b)
(c)
(d)
(e)
(f)
(g)
Refresh
*Nmax-Nmin≧32

FIG. 16

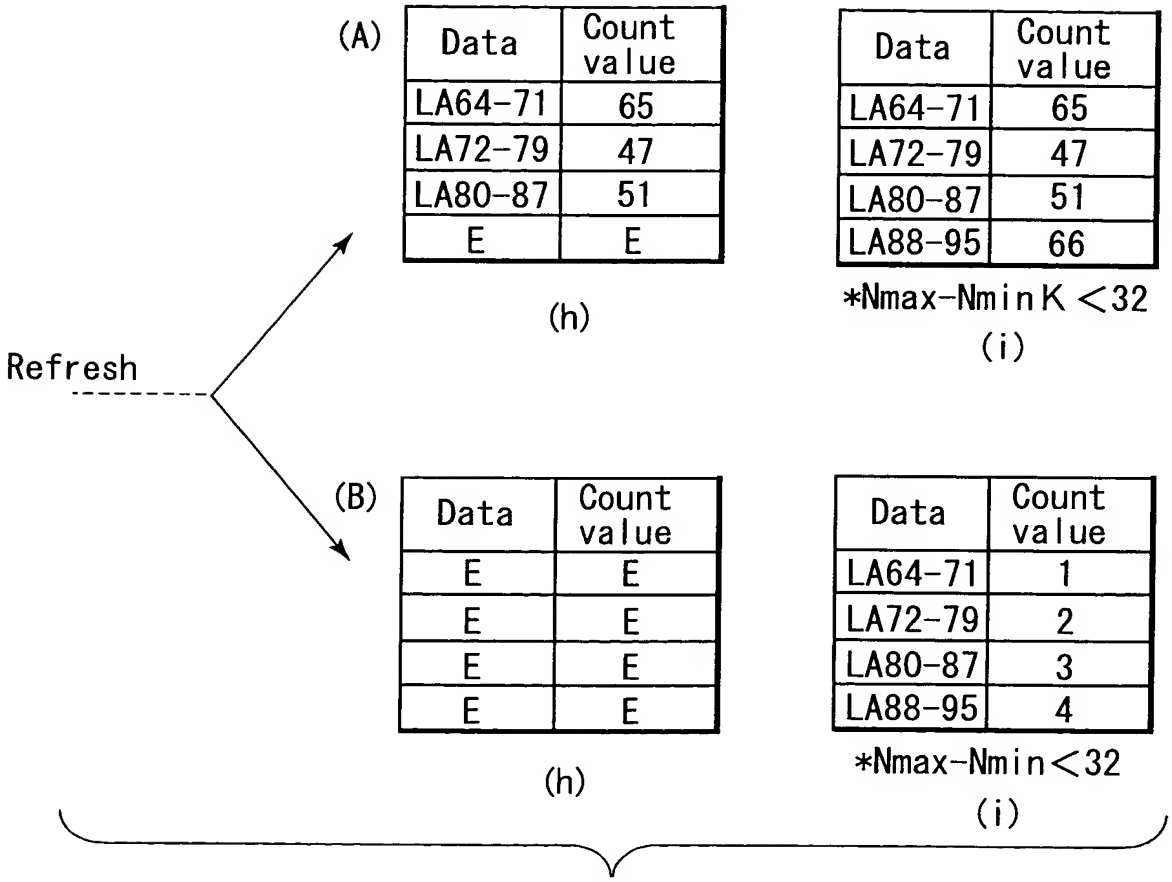
(A)
Data
Count value
LA64-71
65
LA72-79
47
LA80-87
51
E
E
(h)
Data
Count value
LA64-71
65
LA72-79
47
LA80-87
51
LA88-95
66
*Nmax-NminK <32
(i)
Refresh
(B)
Data
Count value
E
E
E
E
E
E
E
E
(h)
Data
Count value
LA64-71
1
LA72-79
2
LA80-87
3
LA88-95
4
*Nmax-Nmin<32
(i)

FIG. 17

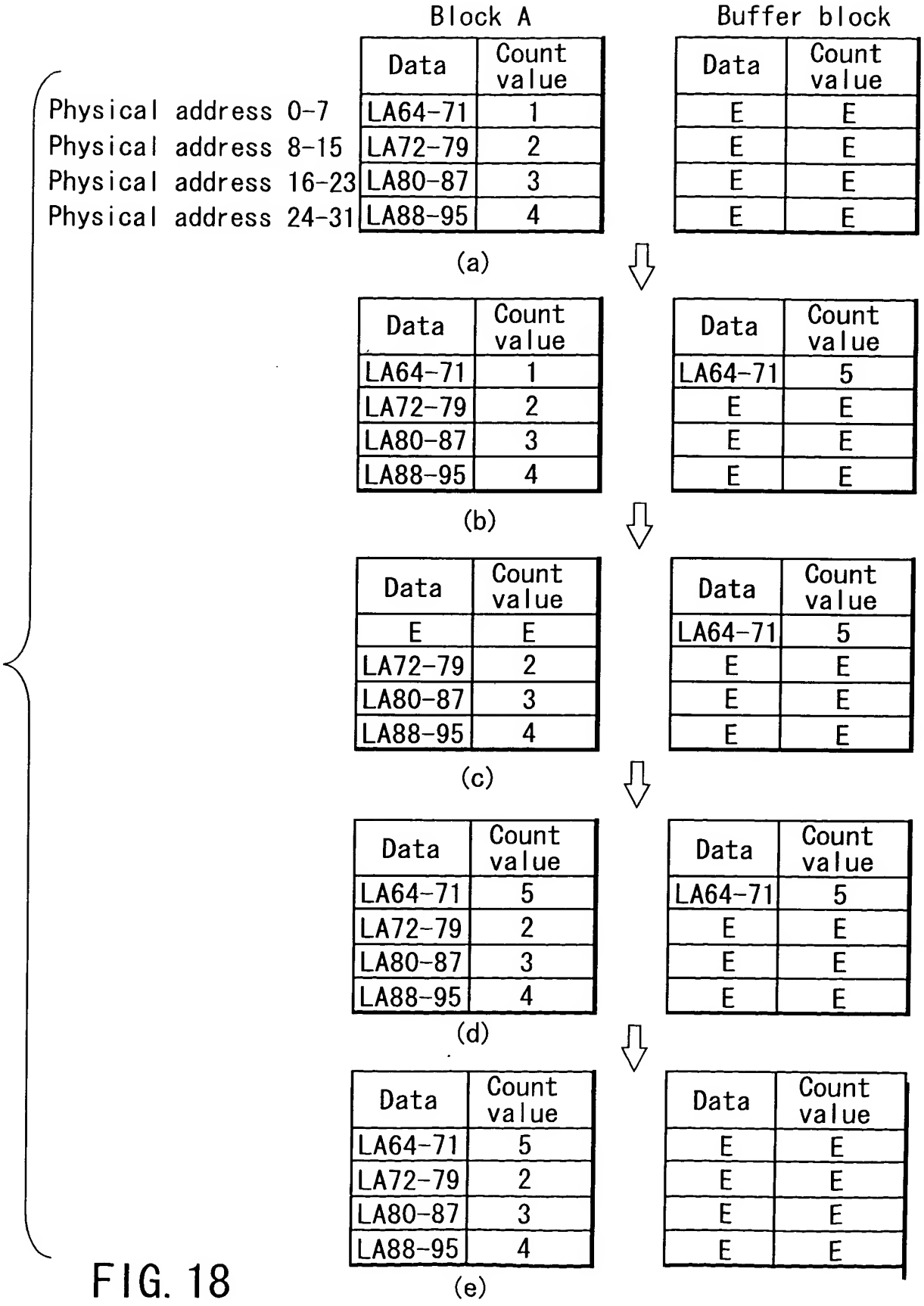
Block A
Buffer block
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
Data
Count value
LA64-71
LA72-79
LA80-87
LA88-95
E
1
2
3
4
5
(a)
(b)
(c)
(d)
(e)

FIG. 18

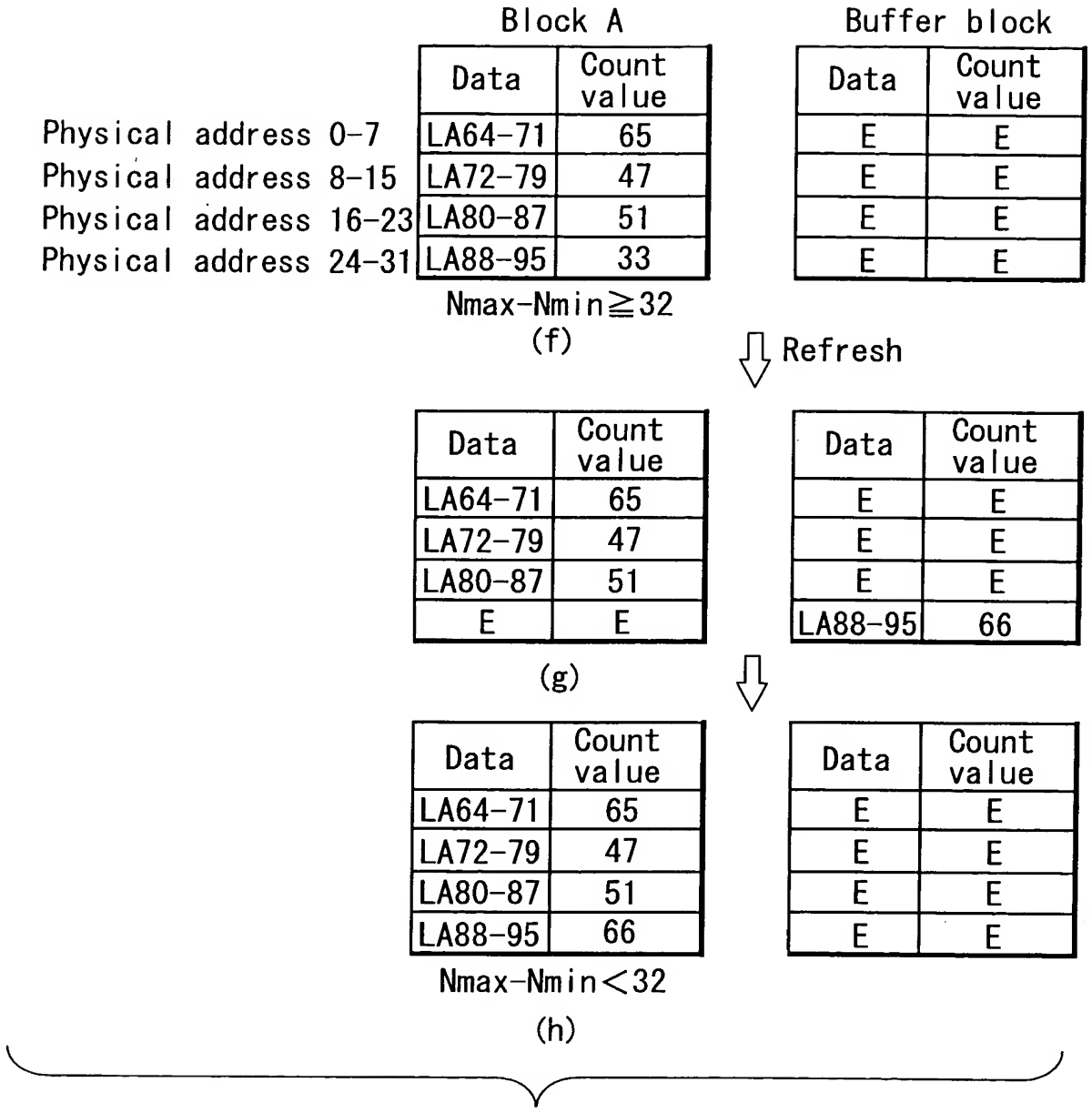
Block A
Buffer block
Data
Count value
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
LA64-71
65
LA72-79
47
LA80-87
51
LA88-95
33
E
E
Nmax-Nmin≧32
(f)
Refresh
LA88-95
66
(g)
Nmax-Nmin<32
(h)

FIG. 19

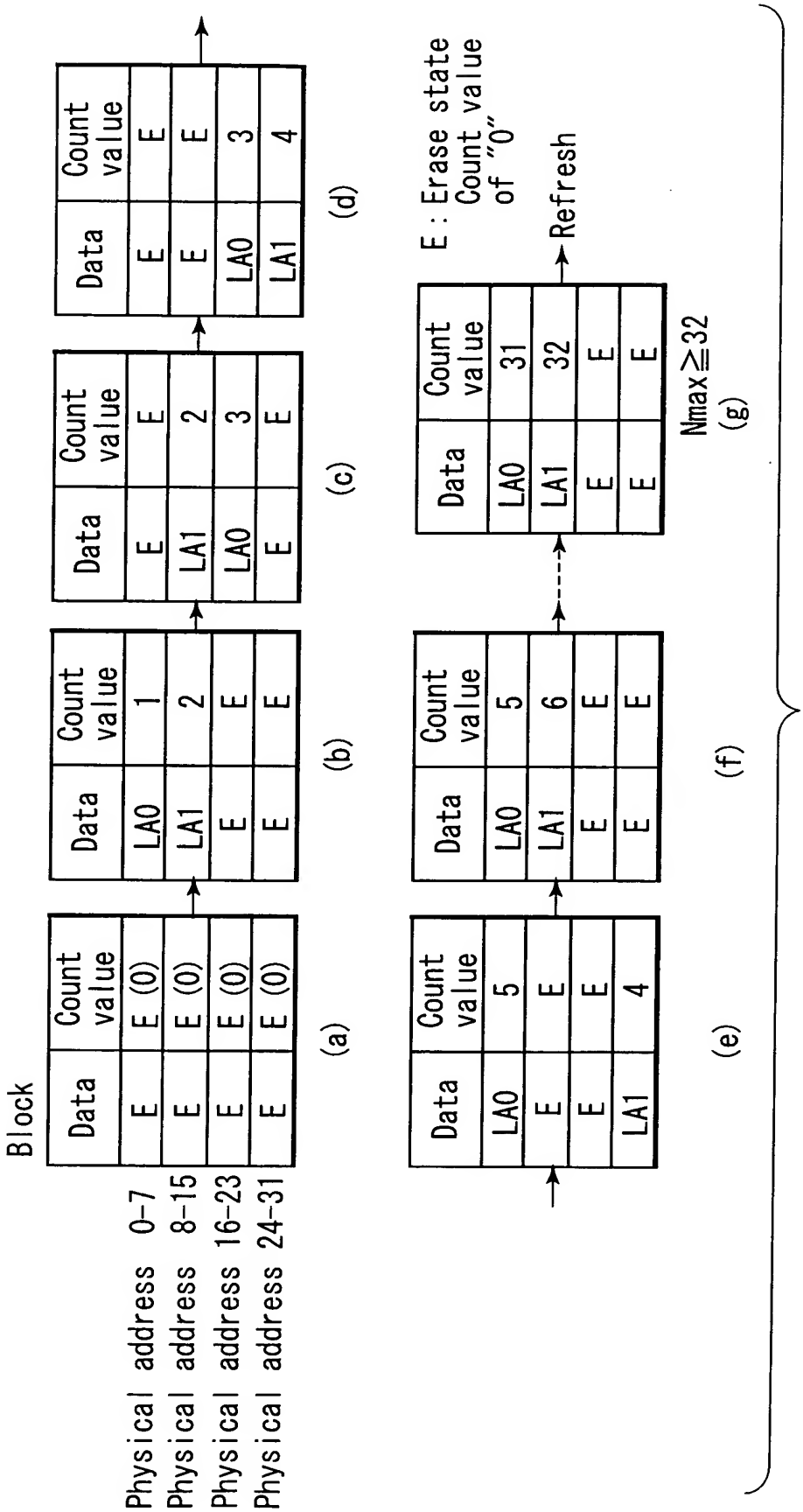
Block
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
Data
Count value
E (0)
LA0
LA1
E
1
2
3
4
5
6
31
32
(a)
(b)
(c)
(d)
(e)
(f)
(g)
E : Erase state
Count value of "0"
Refresh
Nmax≧32

FIG. 20

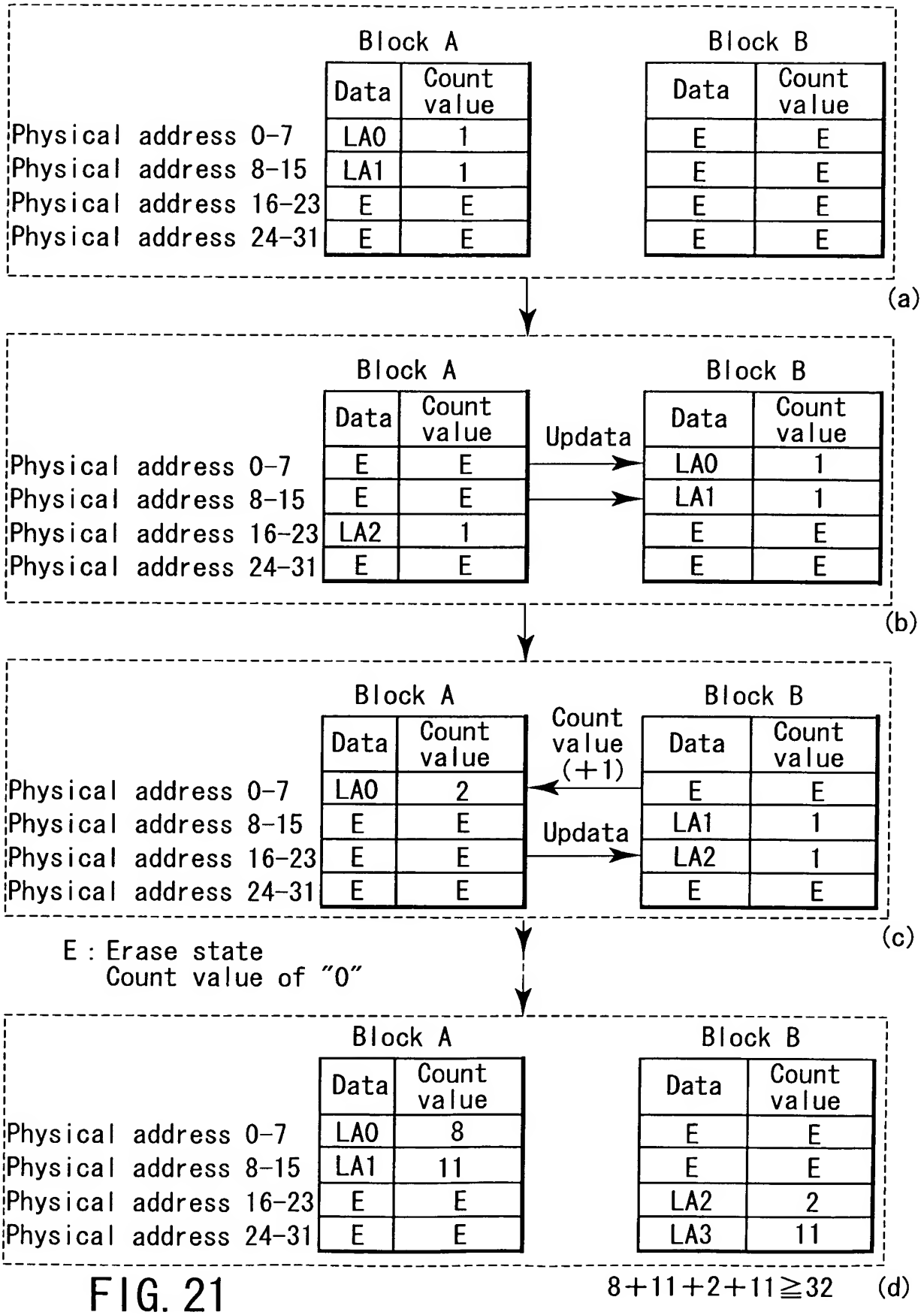
Block A
Block B
Data
Count value
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
LA0
LA1
LA2
LA3
E
1
2
8
11
Updata
Count value (+1)
(a)
(b)
(c)
(d)
E : Erase state
Count value of "0"
8+11+2+11≧32

FIG. 21

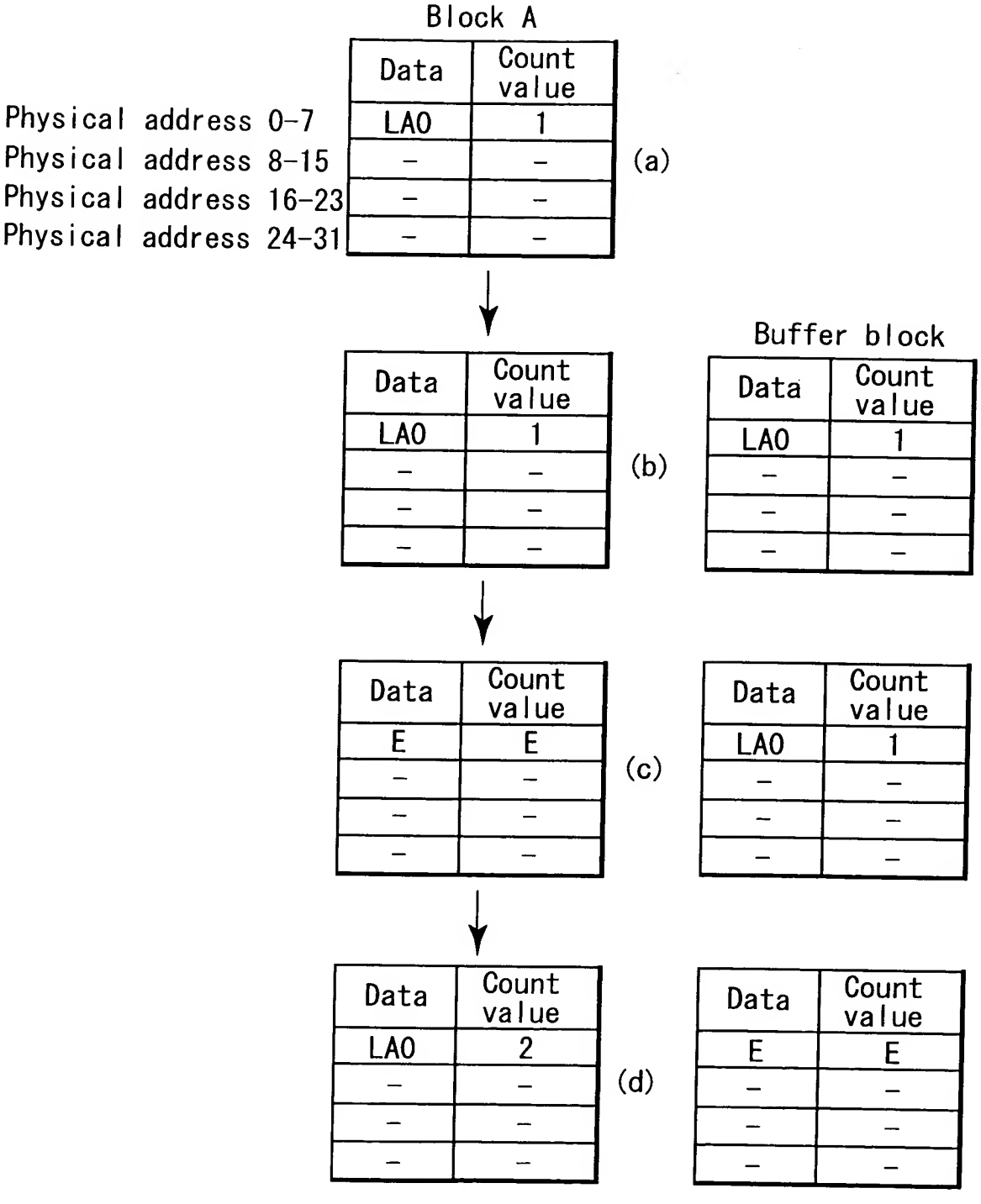
Block A
Data
Count value
Physical address 0-7
Physical address 8-15
Physical address 16-23
Physical address 24-31
LA0
1
(a)
(b)
Buffer block
E
(c)
2
(d)

FIG. 22

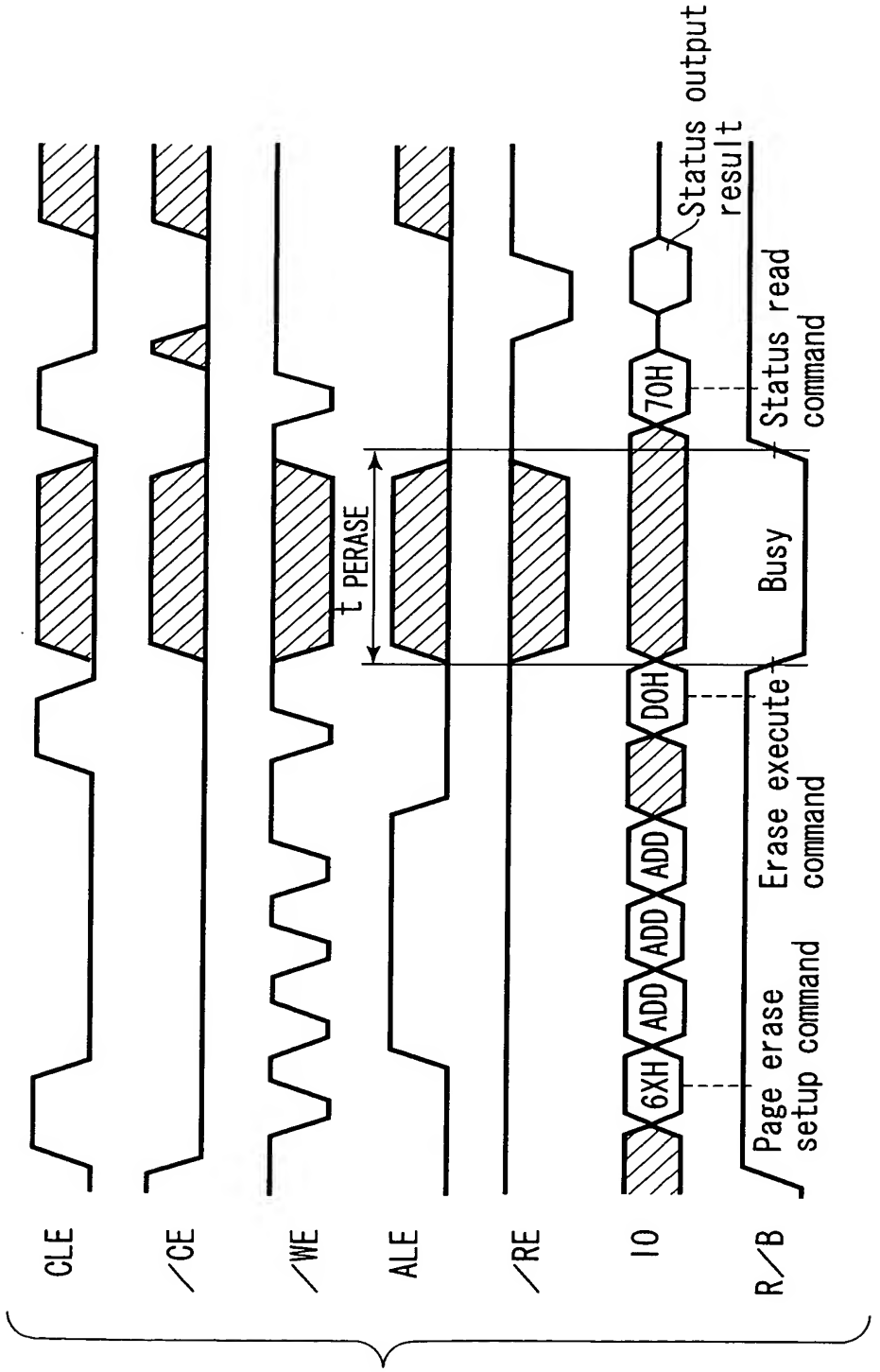
CLE
/CE
/WE
ALE
/RE
IO
R/B
tPERASE
6XH
ADD
ADD
ADD
D0H
70H
Page erase setup command
Erase execute command
Busy
Status read command
Status output result
: VIH or VIL

FIG. 23

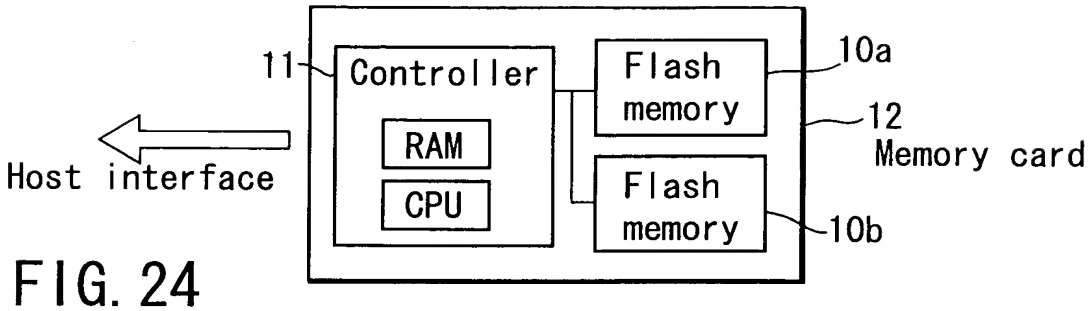

FIG. 24

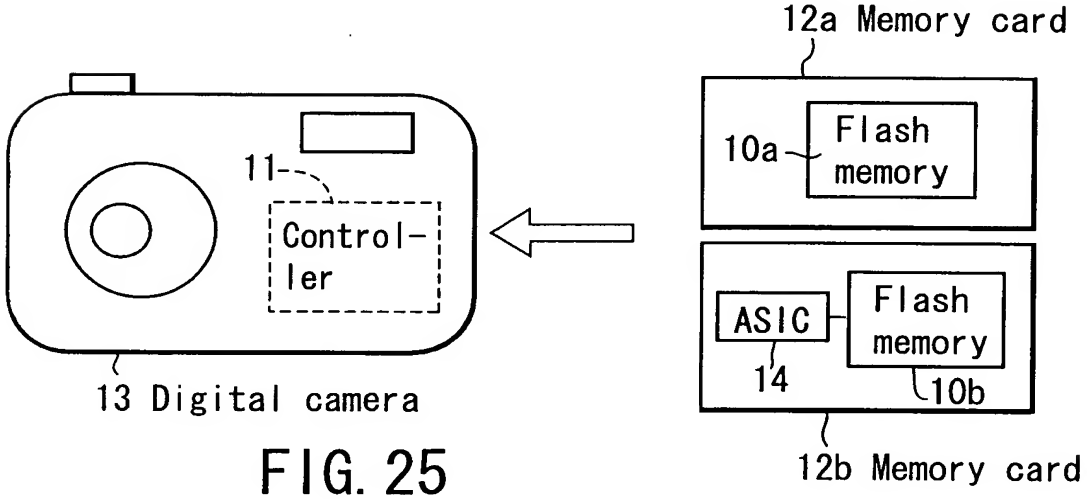

FIG. 25

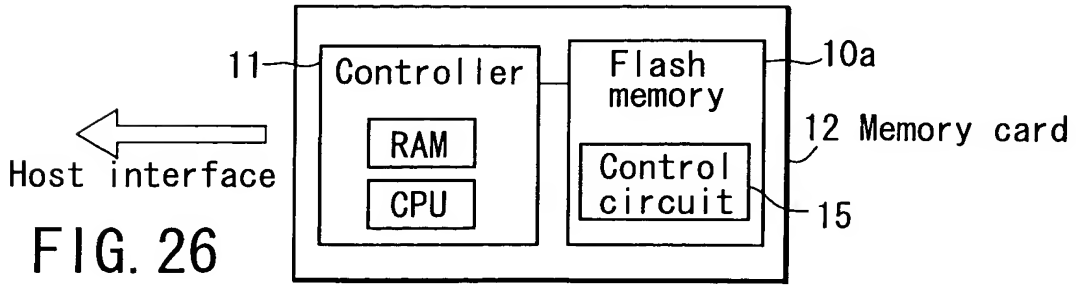

FIG. 26